Product Specification

Product Code : ZOLZOE023

Customer
Approved by Customer
Approved Date:

Designed By	Checked By	Approved By	
		R&D	QA

CONTENT

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
Y01	Initial Release.	2022-09-24	

1. Overview

LZOE023 is a 0.23-inch full-color silicon-based display module with a 640 x 400 lattice. The display module is characterized by high brightness, high contrast, narrow frame, wide viewing Angle, wide temperature range and low power consumption, and is used for head-mounted displays, AR glasses, etc.

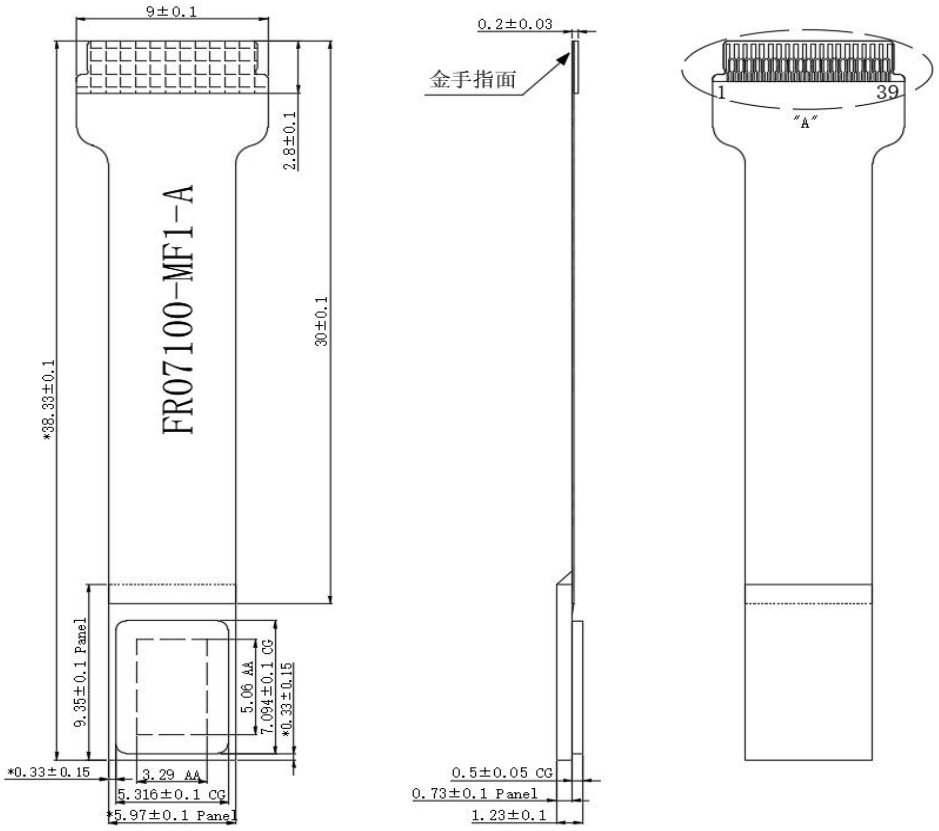
2. Features

- Display Color：Full color
- Small size high-Definition display：0.23" 3255PPI
- Support up to 90hz frame rate.
- Support MIPI input video interface: 2 data lanes/1 clock lanes, speed up to 800M bps
- Support I²C(up to 400K bps) configuration interface
- Operating ambient temperature：-40℃~65℃

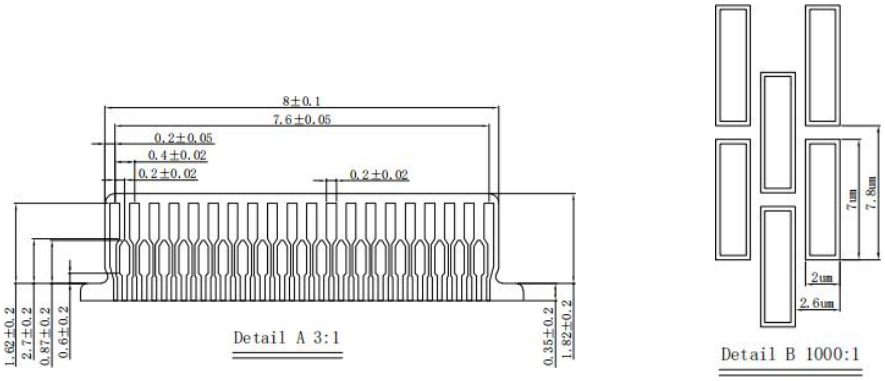
3. Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	640×400	-
2	Dot Size	7.8×7.8	μm^2
3	Active Area	5.06×3.29	mm^2
4	Panel Size	9.35×5.97	mm^2
5	Module Size（FPC）	38.33×9.0	mm^2
6	Diagonal A/A Size	0.23	inch
7	Module Weight	0.2	gram

4. Mechanical Draw



Front view Side view Dorsal view



Connector（39FVXS-RSM1-GAN-TF） pixel size

5. Module Interface

No.	Name	Direction	description
1	VREF	Power	Connect to a 2.2uF capacitor
2	VREGL	Power	Gamma voltage low reference, Connect to a 2.2uF capacitor
3	VREGH	Power	Gamma voltage low reference, Connect to a 2.2uF capacitor
4	AOI_R	In	AOI mode Color R voltage supply , float when normal mode
5	AOI_G	In	AOI mode Color G voltage supply , float when normal mode
6	AOI_B	In	AOI mode Color B voltage supply , float when normal mode
7	AOI_EN	In	AOI mode enable signal, active high(5v), floating or connect to ground when normal mode
8	ELVDD	Power	Pixel reference voltage, Connect to a 2.2uF capacitor
9	VDD50	Power	5.0v power supply
10	VSS	GND	Gound.
11	VDDM	Power	MIPI DPHY power(1.2v), Connect to a 2.2uF capacitor
12	VSSM	GND	Gound.
13	D0P	In/Out	DPHY data lane0 positive signal(double bonding)
14	D0P	In/Out	DPHY data lane0 positive signal(double bonding)
15	D0N	In/Out	DPHY data lane0 negative signal(double bonding)
16	D0N	In/Out	DPHY data lane0 negative signal(double bonding)
17	VSSM	GND	Gound.
18	CLKP	In/Out	DPHY clock lane positive signal(double bonding)
19	CLKP	In/Out	DPHY clock lane positive signal(double bonding)
20	CLKN	In/Out	DPHY clock lane negative signal(double bonding)
21	CLKN	In/Out	DPHY clock lane negative signal(double bonding)
22	VSSM	GND	Gound.
23	D1P	In/Out	DPHY data lane1 positive signal(double bonding)
24	D1P	In/Out	DPHY data lane1 positive signal(double bonding)
25	D1N	In/Out	DPHY data lane1 negative signal(double bonding)
26	D1N	In/Out	DPHY data lane1 negative signal(double bonding)
27	VSSM	GND	Gound.
28	VSS	GND	Gound.
29	VDD18	Power	Core power supply(1.8v)
30	RESETn	In	Whole chip reset pin, active low
31	SCL	In/Out	I²C configuration interface’s clock signal(up to 400kbps)
32	SDA	In/Out	I²C configuration interface’s data signal
33	DEV_ADD R	In	I²C slave address pin, 0: I²C slave address is 8’ha0 1: I²C slave address is 8’ha8
34	TEST_EN	In	Test enable pin, 0: normal mode; 1: scan mode
35	GPIO0	In/Out	General signal 0, it’s for PMIC swire or debug purpose, output swire by default
36	GPIO1	In/Out	General signal 1, it’s for debug purpose, output osc clk by default

37	VPP	Power	Program power for OTP(7.5v), Float when not program OTP
38	VCOM	Power	Power supply for all OLEDs' cathode, its range is from -0.8v to -4v, typical is -2v

6. Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Power supply	VDD50	-0.3	+7.1	V	IC maximum rating
Cathode	VCOM	-4.0	-0.8	V	IC maximum rating
Logical voltage	VDD18	-0.3	+2.1	V	IC maximum rating
Operating Temp	Top	-40	+65	℃	-
Storage Temp	Tstg	-55	+80	℃	-

Note: The maximum range value is the limit value that cannot be exceeded at an instant. Conditions under which these ratings are used or exceeded may affect the life and reliability of the product, but the product may also be damaged. It is recommended to work under typical operating conditions of the product.

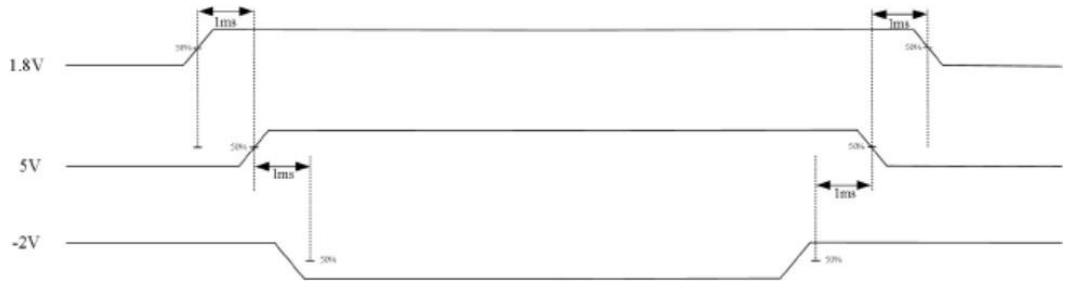
7. Rated operating range

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply voltage	VDD50	-	-	5	-	V
	VCOM	-	-	-2	-	V
	VDD18	-	-	1.8	-	V
High level input voltage	VIH	VDD18=1.65V ~ 1.95V	0.7* VDD18	-	VDD18	V
Low level Input Voltage	VIL	VDD18=1.65V ~ 1.95V	0	-	0.3* VDD18	V
Logic high level output voltage	VOH	Iout = -1mA	0.8* VDD18	-	VDD18	V
Logic low level output voltage	VOL	Iout = +1mA	0	-	0.2* VDD18	V

8. Electro-optical Characteris

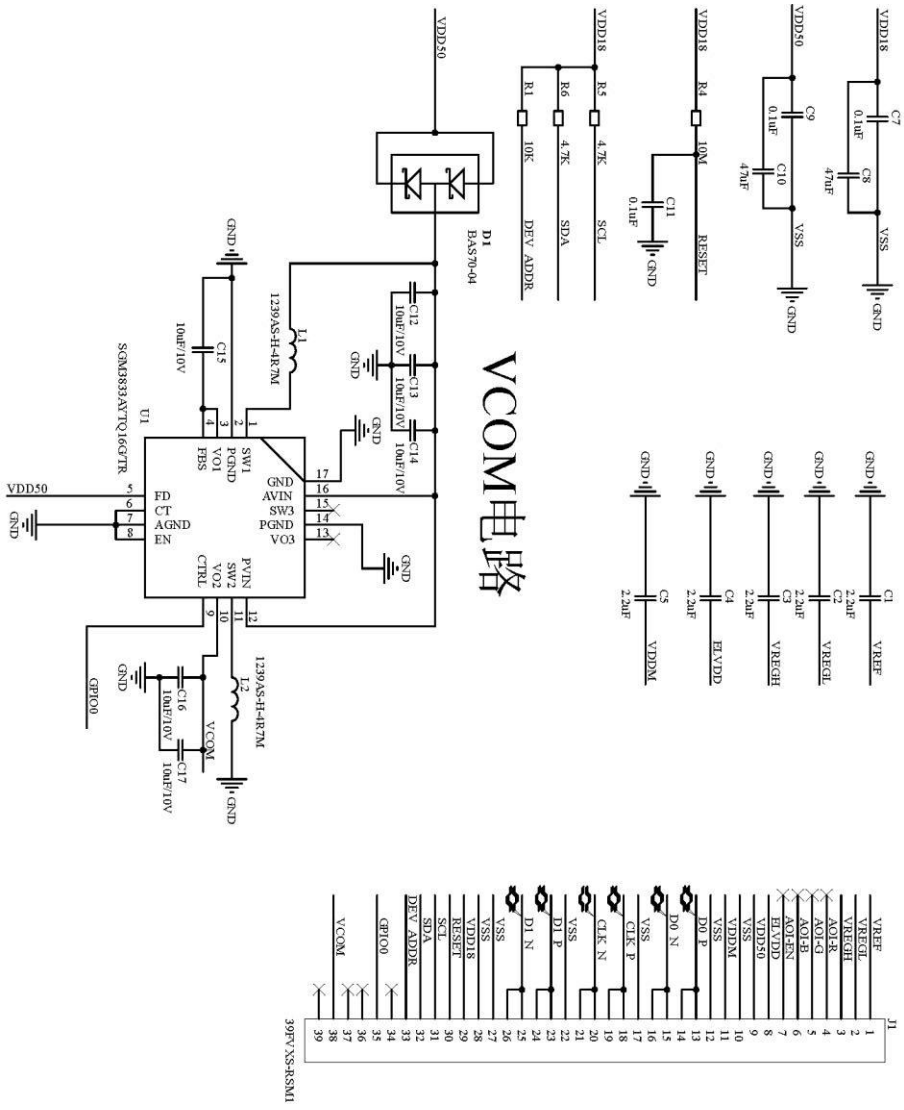
ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode Brightness	Lbr	All pixels ON	-	5000	-	cd/m2
Normal Mode Power Consumption	Pt	All pixels ON	-	250	-	mW
C.I.E（W）	(x)	x,y(CIE1931)	0.30	0.31	0.32	-
	(y)		0.32	0.33	0.34	-
C.I.E（R）	(x)		0.59	0.60	0.61	-
	(y)		0.32	0.33	0.34	-
C.I.E（G）	(x)		0.22	0.23	0.24	-
	(y)		0.62	0.63	0.64	-
C.I.E（B）	(x)		0.13	0.14	0.15	-
	(y)		0.06	0.07	0.08	-
Dark Room Contrast	CR	-	100,000:1	-	-	-

9. Power Supply Sequence



Power On and off Sequences

10. Application circuit



11. Blocks

10.1 MIPI DPHY/DSI Receiver Module

The MIPI receiver is compliant with DPHY1.1 and DSI1.1. It can support up to 800Mbps for each data lane when high speed mode, and supports 10Mbps for low power mode data transmission. It also supports low power mode turn around function. It supports clock stop on D-PHY clock lane for power saving and ultra low-power mode with all data lanes and clock lane power down. There are ECC and CRC for header and payload protection. It can configured to be 1 or 2 data lanes. It supports RGB888 and RGB101010 video format.

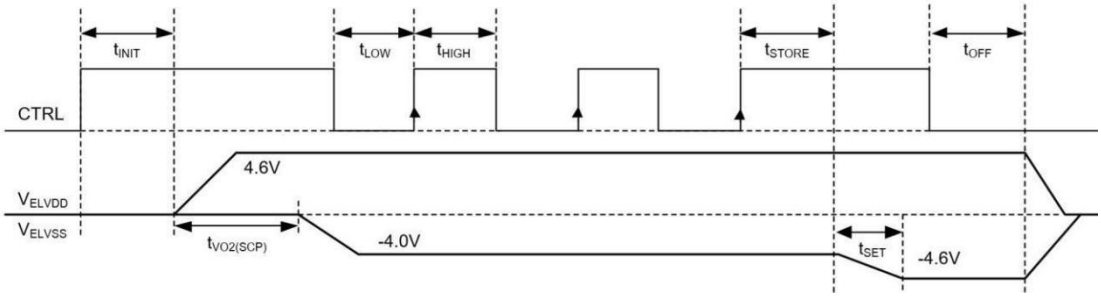
10.2 ABP Bus Matrix

APB bus address mapping, apb bus address signals is 14 bits, there are 2 apb masters, 1 is I²C slave transactions convertor, other is OTP loader. When OTP loader is loading data, I²C slave can't receive any data by stalling SCL to low, after OTP loading finish, then I²C slave can receive data from I²C master. There are 5 apb slave : otp slave(slave id is 4'b0xxx), mipi apb slave(slave id is 4'b1000), system apb slave(slave id is 4'b1001), video process apb slave(slave id is 4'b1010), tcon apb slave(slave id is 4'b1011). APB bus address's 4 highest bits([13:10]) are apb slave id, its 10 lowest bits([9:0]) are this slave's registers address.

10.3 VCOM adjustment

FR07100 uses SWIRE protocol to set the Vcom voltage, swire shares with GPIO0. The Swire timing diagram is as figure 2, CTRL is controlled by swire, VELVSS is Vcom.

Addr(ID:9)	Bits	NAME	W/R	DEFAULT	DESCRIPTION
0xc	5:00	soft_swire_value	W/R	0x1	swire pulse number



Swire timing diagram

10.4 Video Bist

FR07100 has build-in video generation module, it can generate solid color image and color bar pattern, and color bar width is configurable.

Video bist Control Registers：

Addr(ID:A)	Bits	NAME	W/R	DEFAULT	DESCRIPTION
0x50	7	r_video_bist_en	W/R	0x0	0: normal mode; 1: enable video bist module
	6:04	r_video_bist_pattern	W/R	0x0	3'h0: the 1st color bar is white; 3'h1: the 1st color bar is black; 3'h2: the 1st color bar is red; 3'h3: the 1st color bar is green; 3'h4: the 1st color bar is blue; Other value are reserved;
	3:02	Reserved		0x0	
	1:00	r_color_bar_width[9:8]	W/R	0x0	The high 2 bits of r_color_bar_width
0x51	7:00	r_color_bar_width[7:0]	W/R	0x40	The low 8 bits of r_color_bar_width, default value of each color bar's width is 64 pixels

10.5 I² C Slave Interface Module

The I2C slave address is 8'b1010X00Y, bit X value is determined by pin dev_addr_in, and bit Y is read/write flag. I2C slave module support up to 400kpbs speed. It support single byte or multi bytes(up to 256 bytes including 2 bytes of reg address) transfer, the first transfer byte is registers address low byte(reg_addr[7:0]) , the second transfer byte is registers address high byte(reg_addr[13:8], reg_addr[15:14] are reserved). reg_addr[13:10] are apb slave id. I2C slave interface will convert the i2c transactions to APB master transactions, and then connect it to APB bus matrix's apb master 1 interface. Figure 3 show the i2c read/write transaction.

I²C Write/Read Protoca

12. Reliability

NO.	Test Item	Test Condition	Judgement Standard	Remark
1	High temperature storage	Non-working condition of product, test condition: 80℃, 240H. After the test, the product was taken out and returned to room temperature to confirm the situation.	After the test is done, 1. No abnormal appearance 2. No obvious display defects or related malfunctions	
2	High temperature operation	Product working condition, test condition: 65℃, time 240H. After the test is completed, the display function and appearance of the product are checked after the room temperature is restored.		
3	Low temperature storage	Non-working condition of product, test condition: -40℃, 240H. After the test, the product was taken out and returned to room temperature to confirm the situation.		
4	Low temperature operation	Product working condition, test condition: -20℃, time 240H. After the test, the product was taken out and returned to room temperature to confirm the situation.		
5	Thermal shock storage	Test conditions: -30/80℃ high and low temperature each remain for 30min as one cycles, and the conversion time of high and low temperature is less than 5min, a total of 100cycles are made. After the test, the product was taken out and returned to room temperature to confirm the situation.		
6	High temperature and high humidity cycle	The test was carried out for a Cycle (24H) in the following manner, with a total of 10 cycles. 1,The experimental chamber is initially placed at 30℃/90%RH. 2, humidity unchanged, 2H time temperature uniform rise to 60℃. 3, 60℃/90%RH, keep for 6H. 4,The humidity remains unchanged, and the temperature drops to 30℃ at a constant rate in 8H. 5, 30℃/90%RH, keep for 8H. During the last 4 hours of the 30℃/90%RH stage of the fifth cycle, the internal energy check was carried out. After the test, the product was taken out and returned to room temperature to confirm the situation again.		